INTEGRATED INTERFACE CIRCUITRY FOR INTEGRATED VRM POWER FIELD EFFECT TRANSISTORS

[0001] The present application is related to U.S. Provisional Application Serial Number 60/432,302, filed on December 10, 2002, and entitled 'Integrated Half-Bridge Circuit.' The disclosure of this application is hereby specifically incorporated herein by references and for all purposes.

Power-converters are often used in power supplies, power amplifiers and motor drives. Down converters, including Buck converters are often used to convert an input voltage to a lower voltage for supplying power to a load, such as a microprocessor. These microprocessors have applicability in personal computers (PC) as well as other electronic devices. In PC applications, the input voltage to the converter is on the order of 12 V, and the required output is on the order of approximately 1.4 V, or a factor of about ten in step-down. Moreover, the required output currents of these converters are increasing to above 50A, further adding to the design considerations of these circuits, and their devices.

[0002] Down-converter circuits often include a control transistor and a synchronous rectifier. These devices are often metal-oxide-semiconductor (MOS) transistors, which are silicon-based field effect transistors (FET). The use of a control FET (CF) and a synchronous rectifier FET (SF) has certain advantages. However, in known circuits these devices are discrete elements or are disposed in modules. Such circuits have certain drawbacks. For example, as the demand for faster switching frequencies increases, parasitic effects in such devices can have a deleterious impact on the ability of the CF and SF to meet these demands.

[0003] The losses associated with the on-and-off switching of down converters are beneficially minimized as much as possible. This has certain benefits, such as improving the battery life within the PC and reduction of the heat-dissipation and minimizing the volume. Conversion loss in MOSFET's is determined partly by resistance and partly by the figure of merit of the device, which is proportional to the on resistance, R_{on}, and the gate-to-drain charge, Q_{gd}.

[0004] Moreover, in PC microprocessor applications, the input voltage is approximately 12 V, and the output voltage is approximately 1.4V. The CF and SF

switches are relatively high in power and speed, also include a relatively large gate input capacitance, which must be switched into an on and off state relatively quickly. To this end, the switching at the gate occurs at periods on the order of nanoseconds, and the attendant switching currents between the gate and the source are significant, being in the order of Amps.

[0005] In many situations, the current drivers for these switches are often remotely located in known devices, and are thus connected to the switches by leads. These lengthy connections further exacerbate inductive effects, and attendant delay due to the time-changing current. This slows down the time rate of change of the voltage at the gate. Furthermore, during the switching to the off-state, an over-shoot ringing may occur. As can be appreciated, the switching of the voltage at the gate can be significantly impeded by these inductive effects.

[0006] What is needed therefore is a power down-converter circuit which overcomes at least the short-comings of the known devices described above.

[0007] In accordance with an example embodiment, a down converter includes an interface section, which connects the down converter to switches and respective driver circuits, wherein the driver circuits and the switches are combined on a common integrated circuit.

[0008] The invention is best understood from the following detailed description when read with the accompanying drawing figures. It is emphasized that the various features are not necessarily drawn to scale. In fact, the dimensions may be arbitrarily increased or decreased for clarity of discussion.

[0009] Fig. 1 is a schematic diagram of a down converter in accordance with an example embodiment.

[00010] Fig. 2a is a cross-sectional view (High-side) of an integrated circuit of a driver circuit and switches in accordance with an example embodiment.

[00011] Fig. 2b is a cross-sectional view (Low-side) of an integrated circuit of a driver circuit and switches in accordance with an example embodiment.

[00012] Fig. 3 is a level shifter in accordance with an example embodiment.

[00013] In the following detailed description, for purposes of explanation and not limitation, exemplary embodiments disclosing specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one having ordinary skill in the art having had the benefit of the present

disclosure, that the present invention may be practiced in other embodiments that depart from the specific details disclosed herein. Moreover, descriptions of well-known devices, methods and materials may be omitted so as to not obscure the description of the present invention.

[00014] Fig. 1 is a schematic diagram of a down-converter circuit 100 in accordance with an example embodiment. A simple interface section is integrated on a power chip 101, which includes a high side (HS) switch, and a low side (LS) switch as is well known. The power chip 101 may be of the type described in the above-referenced provisional application. A high side (HS) block 102 is a current driver that drives the HS power device 104. A low side (LS) block 103 is also a current driver that drives the low side (LS) power device 104. Both the HS power device and the LS power device are MOS FET devices, and are of the types described in detail in the provisional application referenced above.

[00015] In accordance with an example embodiment, the integration of the HS block 102 and the LS block 103 reduces the parasitic inductance and the resistance between the respective blocks and the power FET's, thus improving the access time and reducing the risk of gate pull-up by Miller capacitance between drain and gate.

[00016] In known circuits, on a printed circuit board the distance between the driver and Power-FET is 10mm or more, resulting in a parasitic inductor of at least 10nH. Charging the Power-FET's input-capacitance of typically 2nF in 5nsec to 5V means that the current, represented as I=C *dV/dt, is on the order of approximately 2A. A response of 2A in 1 nsec requires a voltage, V=L.di/dt, on the order of approximately 20V additionally over the inductor or else the speed of the device is reduced accordingly. This parasitic inductor is reduced typically on the order of at least a factor of 10 by the integration of the elements in accordance with example embodiments described herein.

[00017] Upon switching to an off-state, the output current of typically 10A or more charges the drain-capacitor of typically 2nF at dV/dt= i/C= 5V/ns. This involves a wanted sink-current at the gate (typically C_{gd} is on the order of approximately 0.5nF) of I=C.dV/dt=2.5A with rapid access and an additional voltage drop well below the Power-FET's threshold-voltage. The integrated driver of the example

embodiments reduces the parasitic inductance and also allows for access to the gate of the Power-FET at multiple locations with low resistance and low delay.

[00018] The down-converter 100 includes a differential sense input for signals from a controller chip to decoder block 106. The down converter 100 also includes a level shifter 107 to the HS block 102 and HS switch (CF); also the LS block 103 with LS switch (SyncFET) may have a level-shifter (not shown). The HS block 102 and the LS block 103 each are supplied from external capacitors 108 and 109, respectively. For the HS switch, the capacitor is also part of a bootstrap circuit. Finally, it is noted that the input to the decoder 106 has a signal ground 110, whereas the rest of the integrated circuit uses a power ground 111.

[00019] Figs. 2a and 2b show the current drivers of an example embodiment monolithically integrated on a common substrate. It is noted that in the example embodiments of Figs. 2a and 2b, the integration is a monolithic integration in silicon. It is noted that other semiconductor materials and technologies, such as SiGe may be used in carrying embodiments. The details of the processing and structures are generally omitted from the description as these are well-known to one skilled in the semiconductor device and processing arts.

[00020] Fig. 2a shows the HS driver block 200 for the HS switch in accordance with an example embodiment. The HS driver 200 is substantially the same as that which was described in connection with the example embodiment of Fig. 1, and the HS switch (also referred to herein as the HS power switch) substantially the same as that described in the above-referenced provisional application. Fig. 2b shows the LS driver block 201 for the LS switch (also referred to herein as the LS power switch) in accordance with an example embodiment. The LS driver block 201 is substantially the same as that which was described in connection with the example embodiment of Fig. 1, and the LS switch substantially the same as that described in the above-referenced provisional application. Finally, it is noted that the HS driver block and the LS driver block of the example embodiments of Figs. 2a and 2b beneficially are provided on a common substrate (the same integrated circuit), which in the example embodiments described herein is a highly n-doped silicon substrate. In the present discussion these are separated for purposes of clarity.

[00021] Turning initially to Fig. 2a, the HS driver block is shown. The HS block 200 is a CMOS block, which comprises a power NMOS stage 202 and a power

PMOS stage 203; the 'ground'-sides of this CMOS-block are connected to Output (209-210). The HS CMOS block 200 drives a HS Power FET, which functions as HS Switch 204 as shown. In operation, the PMOS stage 203 charges the gate 206 from the C-boot 205, and an NMOS stage 204 discharges the gate to the output voltage 209 (via heavily doped sinker 210), which is here illustratively given at +12 V. In the example embodiment, the substrate 211 is heavily doped as well, and provides the connection to the p-well 212 of the HS switch.

[00022] As described herein, the HS CMOS block 200 needs a high-side latch circuit that is driven by a level shifter; this level-shifter adapts the 5V-signals related to power-ground from the decoder to 5V signals between Gate and Source related to the source of the HS-switch which jumps up and down according to the output-voltage "Out". Moreover, the HS CMOS block requires an external bootstrap capacitor and a (25V) bootstrap diode, which is indicated in Fig.1 . As a diode is difficult to integrate , an external diode (not shown) is required.

[00023] In an example embodiment shown in Fig. 2b the LS CMOS block 201 drives an LS Power FET gate 212 of an LS Switch 213, both relative to power-ground. The LS CMOS block 201, like the HS CMOS block 200 includes an NMOS stage 214 and a PMOS stage 215. The 'ground'-side of this CMOS-block (p-well 216) of the LS driver 218 is connected to a power ground 219. The n^+ substrate 211 ("Out") moves between +12V and Zero and can also for a short time be at approximately - 0.1 V, but must remain less than - 0.7 V relative to the p-well 216 if the LS Power FET (LS Switch 213) is not yet switched on. This latter situation will create conduction in parasitic diodes which are part of a parasitic NPN structure (NMOS drain, PMOS well), which involves additional dissipation and charge collection in the integrated circuit. This must be restricted to minimum by a quick turn-on of the LS power-switch. Finally, the LS CMOS block 201 also beneficially may have a capacitor and even may have a level shifter in case of large voltage-differences in the ground-rail.

[00024] As referenced before, parasitic currents can arise during operation of the down-converters of example embodiments thus described. In the example embodiment of Figs. 2a and 2b, if the HS switch 204 is in an on-state, the substrate 211 is charged to 12 V, and current flows in the load inductance of the down-converter. If the HS switch 204 is in an off-state, the load inductance pulls the

substrate 211 to between -0.1 V and -0.7 V, depending upon the turn-on time of the LS switch 213. This can result in spike diode currents to the p-well of the NMOS and PMOS stages, since the p-wells are connected to the power-ground 219.; this also can create spikes in NPN conduction.

[00025] In Fig.1, a HS level shifter 107 requires a relatively high voltage NMOS device, of approximately 25V; an example embodiment is shown in Fig. 3. The HS level shifter 300 may be disposed on a common substrate with the HS and LS blocks and Power FET's described above. This may be fabricated in an integrated fashion with the NMOS structure 301 in a p-type well 303, where the PMOS n-well 302 functions as the drift region for the NMOS drain 304. If the source/p-well is connected to a signal-ground, which is the input from the controller, it can create issues if the signal-ground differs by several volts from the power-ground due to inductance. In an example embodiment, a different drive is implemented from the input decoder. The source/p-well of the level shift are illustratively connected to the power ground and have the same problem described in conjunction with the LS CMOS block.

[00026] In this example embodiment, the input decoder must split the signals for the LS and HS CMOS blocks (200 and 201) for break-before-make timing. In an example embodiment, a differential signal sense may be used for the input from the controller. Illustratively, this may be effected using a PMOS device, which senses a difference between a VRM signal line and a signal-ground line. The two lines are then connected to a source and gate of a PMOS stage in an example embodiment. The difference is obtained in the drain current of the PMOS stage. This is converted to a Gate-to-Source (GS) signal for the transistor of the level-shifter circuit by a resistor between the gate and the source. This accounts for differences between the local power ground and the signal ground at the controller, taken at the central voltage sensing point.

[00027] The invention being thus described, it would be obvious that the same may be varied in many ways by one of ordinary skill in the art having had the benefit of the present disclosure. Such variations are not regarded as a departure from the spirit and scope of the invention, and such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims and their legal equivalents.